## AMENDMENTS TO THE CLAIMS

Please cancel Claims 17-34 without prejudice. Claims 1-16 remain as previously pending.

1. (Original) A semiconductor device comprising:

a transistor having a source and a drain comprising a substrate material and having a gate trench between the source and the drain; and

an isolation trench filled with a nonconductive material surrounding the transistor,

wherein the gate trench has sidewalls comprising the nonconductive material, which are substantially free of the substrate material.

2. (Original) The device of Claim 1, wherein the substrate material comprises silicon.

3. (Original) The device of Claim 1, wherein the gate trench has a depth within the range of about 50 nm to about 300 nm.

4. (Original) The device of Claim 1, wherein the gate trench has a rounded bottom.

5. (Original) The device of Claim 1, wherein the isolation trench has a depth within the range of about 300 nm to about 500 nm.

6. (Original) The device of Claim 1, wherein the nonconductive material comprises an oxide material.

7. (Original) The device of Claim 1, further comprising a ridge of substrate material between the transistor and the isolation trench, wherein the transistor is separated from the ridge of substrate material by a separation trench filled with the nonconductive material.

8. (Original) The device of Claim 7, wherein the separation trench completely surrounds the source and the drain such that the source and the drain do not contact the ridge of substrate material.

9. (Original) The device of Claim 7, wherein the separation trench is configured such that one side of the source and one side of the drain are in contact with the ridge of substrate material.

10. (Original) An integrated circuit transistor comprising:

a source;

a drain; and

a gate trench between the source and the drain, the gate trench having nonconductive sidewalls and having a first depth,

wherein the transistor is surrounded by an isolation trench having a second depth that is greater than the first depth, and

wherein the nonconductive sidewalls of the gate trench are formed at a point toward the middle of the gate trench and away from the isolation trench.

11. (Original) The transistor of Claim 10, wherein the first depth falls within the range of about 50 nm to about 300 nm.

12. (Original) The transistor of Claim 10, wherein the gate trench has a rounded bottom.

13. (Original) The transistor of Claim 10, wherein the second depth falls within the range of about 300 nm to about 500 nm.

14. (Original) The transistor of Claim 10, further comprising a ridge of substrate material between the transistor and the isolation trench, wherein the transistor is separated from the ridge of substrate material by a separation trench.

15. (Original) The transistor of Claim 14, wherein the separation trench completely surrounds the source and the drain such that the source and the drain do not contact the ridge of substrate material.

16. (Original) The transistor of Claim 14, wherein the separation trench is configured such that one side of the source and one side of the drain are in contact with the ridge of substrate material.

17. – 34. (Canceled)